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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/399,995	PARK, SANG-SIK	
	Examiner	Art Unit	
	Justin P Misleh	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 4 - 20, and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4, 7 – 9, 11 – 15, 17 – 20, and 22* is/are rejected.

7)☒ Claim(s) *5,6,10 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed August 8, 2005 have been fully considered but they are not persuasive.

2. Applicant argues, "the cited figure 1 of Garfinkel shows a charge sensing circuit in which a capacitor C_{FB} is connected between the output of a differential amplifier 23 and the *signal input terminal* of a source follower circuit 25. In contrast, Claim 1 recites 'an output capacitively connected to ***a bias terminal*** of said input source follower circuit,' Claim 14 recites 'a feedback circuit connected to said output terminal and to said input source follower circuit and operative to variably couple the power source and ***the bias terminal*** via a capacitor,' and claim 20 recites 'an output capacitively coupled to ***a bias terminal*** of said input source follower circuit." Hynecek and Garfinkel, alone or in combination, do not disclose these recitations of Claims 1, 14, and 20.

3. Applicant's arguments are erroneous. The Non-Final Office Action (mailed January 27, 2005) made abundantly clear that the Examiner considered the gate of the input source follower circuit to be the bias terminal of the input source follower. On page 3 of the Office Action, the Examiner explicitly stated, "Transistor 54 is part of the input source follower circuit; wherein the gate of transistor 54 is a bias terminal of the input source follower circuit." As admitted by Applicant, "the cited figure 1 of Garfinkel shows a charge sensing circuit in which a capacitor C_{FB} is connected between the output of a differential amplifier 23 and the *signal input terminal* of a source follower circuit 25." The so-called "*signal input terminal*" of the source follower circuit 25, as identified

by Applicant, is in-fact the gate 29 of transistor 26. Hence, Applicant effectively admits that Hynecek in view of Garfinkel discloses the recitations of Claims 1, 14, and 20 including an output capacitively connected to ***a bias terminal*** of said input source follower circuit.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1, 4, 7 – 9, 11 – 15, 17 – 20, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hynecek in view of Garfinkel et al.

6. For **Claim 1**, Hynecek discloses, as shown in figure 2 and as stated in columns 1 (lines 10 – 16 and 60- 67) and 2 (lines 1 – 33), an output-compensated buffer (see figure 2), comprising:

a buffer circuit (see figure 2) that receives an input signal (received from circuit 55 and applied to the gate of transistor 52) and produces an output signal responsive thereto at an output terminal (62), said buffer circuit (figure 2) including an input source follower circuit (52) that receives the input signal (from circuit 55); and

a feedback circuit having an input connected to said output terminal (62) and an output connected to a bias terminal (Transistor 54 is part of the input source follower circuit; wherein the gate of transistor 54 is a bias terminal of the input source follower circuit.) of said input source follower circuit and operative to vary an input of said source

follower circuit responsive to the output signal at said output terminal (see column 2, lines 22 – 32).

While Hynecek disclose the feedback loop stated above, Hynecek does not disclose that the feedback includes a capacitor therein so as to capacitively couple the buffer circuit output to the buffer circuit input. In other words, Hynecek does not disclose varying the input capacitance of the source follower circuit.

On the other hand, Garfinkel et al. also provides a charge detection buffer. More specifically, Garfinkel et al. disclose, as shown in figure 1 and as stated in columns 2 (lines 7 – 10, 28 – 30, and 54 – 68), 3 (lines 1 – 11 and 62 – 68), 4 (line 1), and 6 (lines 11 – 18), a buffer comprised of a feedback circuit (24) beginning at an output terminal (38) of a buffer circuit (20) and ending at an input terminal (19) of the buffer circuit (20), wherein the input terminal (19) is the input of a source follower circuit (25) and feedback circuit (24) is capacitively coupled (by means of capacitor C_{FB}) to the input so as to vary the input capacitance of the source follower (25) response to the output at the output terminal (38).

In summary, as stated in columns 1 (lines 10 – 13) and 6 (lines 11 – 18), at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have include a capacitively coupled feedback circuit, as taught by Garfinkel et al., in the output compensated buffer, disclosed by Hynecek, as a means for enabling small signal currents to be detected in the presence of very large background currents while ensuring the linearity of the circuit.

7. As for **Claim 4**, Hynecek discloses, an output-compensated buffer according to Claim 1, wherein said feedback circuit (circuit path beginning at the output terminal 62

and ending at transistor 52, wherein the path is intercepted with a power source VDD and a resistor 64) is operative to couple the bias terminal (the drain of the circuit 52) to the power source (VDD) responsive to the output signal at the output terminal (62).

As stated above, Garfinkel et al. teach how the feedback is capacitively coupled so as to variably capacitively couple the feedback circuit to the bias terminal.

8. As for **Claim 7**, Hynecek discloses, an output-compensated buffer according to Claim 1, wherein said source follower circuit (52) comprises:

a first transistor (52) having a source terminal, a gate terminal configured to receive the input signal (from circuit 55), and a drain terminal connected to the power source (VDD) through a resistor (64); and

a second transistor (54) having a drain terminal connected to the source terminal of the first transistor (by means of the node supplying an input signal to the circuit 50), a source terminal connected to a signal ground (clearly shown in figure 2) and a gate terminal configured to receive a control signal (initially, a gate terminal of a transistor is always configured to receive a control signal as it the means that controls the transistor; moreover a control signal is supplied constant current source 60); and

wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) is coupled to the drain terminal of said first transistor.

9. As for **Claim 8**, Hynecek discloses, an output-compensated buffer according to Claim 7, wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) is coupled the bias terminal (the drain of the circuit 52).

As stated above, Garfinkel et al. teach how the feedback is capacitively coupled so as to variably capacitively couple the feedback circuit to the bias terminal.

10. As for **Claim 9**, Hynecek discloses, an output-compensated buffer according to Claim 8, wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) is operative to couple the bias terminal (the drain of the circuit 52) to the power source (VDD) responsive to the output signal at the output terminal (62).

As stated above, Garfinkel et al. teach how the feedback is capacitively coupled so as to variably capacitively couple the feedback circuit to the bias terminal.

11. As for **Claim 11**, Hynecek discloses, an output-compensated buffer according to Claim 1, wherein the output terminal (62) of the buffer circuit (see figure 2) is an output terminal of the source follower circuit.

12. As for **Claim 12**, Hynecek discloses, an output-compensated buffer according to Claim 1, wherein the buffer circuit (figure 2) further comprises a source follower circuit (54) connected to an output (the output and the source of the circuit 52 and the drain of the circuit 54 are the same node) of the input follower circuit (52) and operative to produce the output signal responsive to the inputs signal (from circuit 55) applied the input source follower circuit (52).

13. As for **Claim 13**, Hynecek discloses, an output-compensated buffer according to Claim1, in combination with a CCD image capture device (inherent; see explanation below), wherein the CCD image capture device includes a horizontal transfer section that generates the input signal (included in the inherency above).

While Hynecek does not show the details of a CCD imager, the amplifier disclosed by Hynecek clearly designed for and directly used by CCD imager sensors. Therefore, it is inherent that a CCD exists and includes the horizontal transfer section; otherwise, the amplifier of Hynecek would be rendered inoperable.

14. As for **Claim 18**, Hynecek discloses, an output-compensated buffer according to Claim13, wherein the buffer circuit (figure 2) further comprises a source follower circuit (54) connected to an output (the output and the source of the circuit 52 and the drain of the circuit 54 are the same node) of the input follower circuit (52) and operative to produce the output signal responsive to the inputs signal (from circuit 55) applied the input source follower circuit (52).

15. For **Claim 14**, Hynecek discloses, as shown in figure 2 and as stated in columns 1 (lines 10 – 16 and 60- 67) and 2 (lines 1 – 33), an output-compensated buffer (see figure 2), comprising:

a buffer circuit (see figure 2) that receives an input signal (from circuit 55) and produces an output signal responsive thereto at an output terminal (62), said buffer circuit (figure 2) including an input source follower circuit (52) that receives a bias voltage from a power source (VDD); and

a feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) connected to said output terminal (62, by means of circuit 50) and to said input source follower circuit (by means of the drain of the circuit 52) and operative to couple the power source (VDD) and the bias terminal (the drain of circuit 52).

While Hynecek disclose the feedback loop stated above, Hynecek does not disclose that the feedback includes a capacitor therein so as to capacitively couple the buffer circuit output to the buffer circuit input. In other words, Hynecek does not disclose varying the input capacitance of the source follower circuit via a capacitor.

On the other hand, Garfinkel et al. also provides a charge detection buffer. More specifically, Garfinkel et al. disclose, as shown in figure 1 and as stated in columns 2 (lines 7 – 10, 28 – 30, and 54 – 68), 3 (lines 1 – 11 and 62 – 68), 4 (line 1), and 6 (lines 11 – 18), a buffer comprised of a feedback circuit (24) beginning at an output terminal (38) of a buffer circuit (20) and ending at an input terminal (19) of the buffer circuit (20), wherein the input terminal (19) is the input of a source follower circuit (25) and feedback circuit (24) is capacitively coupled (by means of capacitor C_{FB}) to the input so as to vary the input capacitance of the source follower (25) response to the output at the output terminal (38).

In summary, as stated in columns 1 (lines 10 – 13) and 6 (lines 11 – 18), at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have include a capacitively coupled feedback circuit, as taught by Garfinkel et al., in the output compensated buffer, disclosed by Hynecek, as a means for enabling small signal currents to be detected in the presence of very large background currents while ensuring the linearity of the circuit.

16. As for **Claim 15**, Hynecek discloses, an output-compensated buffer according to Claim 14, wherein said source follower circuit (52) comprises:

a first transistor (52) having a source terminal, a gate terminal configured to receive the input signal (from circuit 55), and a drain terminal connected to the power source (VDD) through a resistor (64); and

a second transistor (54) having a drain terminal connected to the source terminal of the first transistor (by means of the node supplying an input signal to the circuit 50), a source terminal connected to a signal ground (clearly shown in figure 2) and a gate terminal configured to receive a control signal (initially, a gate terminal of a transistor is always configured to receive a control signal as it the means that controls the transistor; moreover a control signal is supplied constant current source 60); and

wherein said feedback circuit (circuit path beginning at the drain of the circuit 50 and ending at the drain of the circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64) is coupled to the drain terminal of said first transistor.

17. As for **Claim 17**, Hynecek discloses, an output-compensated buffer according to Claim 14, wherein the output terminal (62) of the buffer circuit (see figure 2) is an output terminal of the source follower circuit.

18. As for **Claim 19**, Hynecek discloses, an output-compensated buffer according to Claim14, in combination with a CCD image capture device (inherent; see explanation below), wherein the CCD image capture device includes a horizontal transfer section that generates the input signal (included in the inherency above).

While Hynecek does not show the details of a CCD imager, the amplifier disclosed by Hynecek clearly designed for and directly used by CCD imager sensors. Therefore, a CCD must exist and includes the horizontal transfer section; otherwise, the amplifier of Hynecek would be rendered inoperable.

19. For **Claim 20**, Hynecek discloses, as shown in figure 2 and as stated in columns 1 (lines 10 – 16 and 60- 67) and 2 (lines 1 – 33), an image capture device, comprising:

a charged coupled device (CCD) that generates a video signal (see explanation below);

a buffer circuit (see figure 2) responsive to the CCD and operative to receive the video signal (received from circuit 55 and applied to the gate of transistor 52) and produces an output signal responsive thereto at an output terminal (62), said buffer circuit (figure 2) including an input source follower circuit (52) that receives the input signal (from circuit 55); and

a feedback circuit having an input connected to said output terminal (62) and an output connected to a bias terminal (Transistor 54 is part of the input source follower circuit; wherein the gate of transistor 54 is a bias terminal of the input source follower circuit.) of said input source follower circuit and operative to vary an input of said source follower circuit responsive to the output signal at said output terminal (see column 2, lines 22 – 32).

While Hynecek does not show the details of a CCD imager, the amplifier disclosed by Hynecek clearly designed for and directly used by CCD imager sensors. Therefore, a CCD must exist; otherwise, the amplifier of Hynecek would be rendered inoperable.

Furthermore, while Hynecek disclose the feedback loop stated above, Hynecek does not disclose that the feedback includes a capacitor therein so as to capacitively couple the buffer circuit output to the buffer circuit input. In other words, Hynecek does not disclose varying the input capacitance of the source follower circuit.

On the other hand, Garfinkel et al. also provides a charge detection buffer. More specifically, Garfinkel et al. disclose, as shown in figure 1 and as stated in columns 2 (lines 7 – 10, 28 – 30, and 54 – 68), 3 (lines 1 – 11 and 62 – 68), 4 (line 1), and 6 (lines 11 – 18), a buffer comprised of a feedback circuit (24) beginning at an output terminal (38) of a buffer circuit (20) and ending at an input terminal (19) of the buffer circuit (20), wherein the input terminal (19) is the input of a source follower circuit (25) and feedback circuit (24) is capacitively coupled (by means of capacitor C_{FB}) to the input so as to vary the input capacitance of the source follower (25) response to the output at the output terminal (38).

In summary, as stated in columns 1 (lines 10 – 13) and 6 (lines 11 – 18), at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have include a capacitively coupled feedback circuit, as taught by Garfinkel et al., in the output compensated buffer, disclosed by Hynecek, as a means for enabling small signal currents to be detected in the presence of very large background currents while ensuring the linearity of the circuit.

20. As for **Claim 22**, Hynecek discloses, an output-compensated buffer according to Claim 1, wherein said feedback circuit (circuit path beginning at the output terminal 62 and ending at transistor 52, wherein the path is intercepted with a power source VDD and a resistor 64) is operative to couple the bias terminal (the drain of the circuit 52) to the power source (VDD) responsive to the output signal at the output terminal (62).

As stated above, Garfinkel et al. teach how the feedback is capacitively coupled so as to variably capacitively couple the feedback circuit to the bias terminal.

Allowable Subject Matter

21. **Claims 5, 6, 10, and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. As for **Claims 5 and 16**, while the prior art teaches of an output-compensated buffer comprised of a buffer circuit including an input source follower circuit that receives an input signal and a feedback circuit connected to an output terminal and to the input source follower circuit that is operative to vary an input capacitance of the source follower circuit wherein the bias terminal of the input source follower circuit is coupled to a power source and wherein the feedback circuit is variably capacitively coupled the power source and the bias terminal; however, the prior art does not teach or fairly suggest wherein the feedback circuit comprises a second source follower circuit having an input terminal that receives an output signal output from the input source follower circuit and an output terminal that is coupled to the bias terminal of the input source follower circuit.

23. As for **Claim 10**, while the prior art teaches of an output-compensated buffer comprised of a buffer circuit including an input source follower circuit that receives an input signal and a feedback circuit connected to an output terminal and to the input source follower circuit wherein the input source follower circuit is comprised of a first transistor having a source terminal, a gate terminal configured to receive the input signal, and a drain terminal connected to the power source through a resistor and a second transistor having a drain terminal connected to the source terminal of the first transistor, a source terminal connected to a signal ground and a gate terminal configured to receive a control signal; and wherein said feedback circuit is coupled to the drain terminal of said

first transistor; however, the prior art does not teach or fairly suggest wherein the feedback circuit comprises a third transistor having a source terminal, a drain terminal connected to the power source, and a gate terminal connected to the output terminal of the buffer circuit and a fourth transistor having a drain terminal connected to the source terminal of the third transistor, a drain terminal connected to a signal ground and a gate terminal configured to receive a control signal; and a capacitor coupled between the drain terminal of the fourth transistor and the drain terminal of the first transistor.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Ngoc Yen Vu can be reached on 571.272.7320. The fax phone number for the organization where this application or proceeding is assigned is 571.273.3000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
October 17, 2005

NGOC YEN VU
PRIMARY EXAMINER